2 T825 Circuit Operation

This section provides a basic description of the circuit operation of the T825 receiver.

Refer to Section 6 where the parts lists, grid reference index and diagrams will provide detailed information on identifying and locating components and test points on the main PCB. The parts lists and diagrams for the memory and VCO PCBs are in Part E.

The following topics are covered in this section.

2.1 Introduction

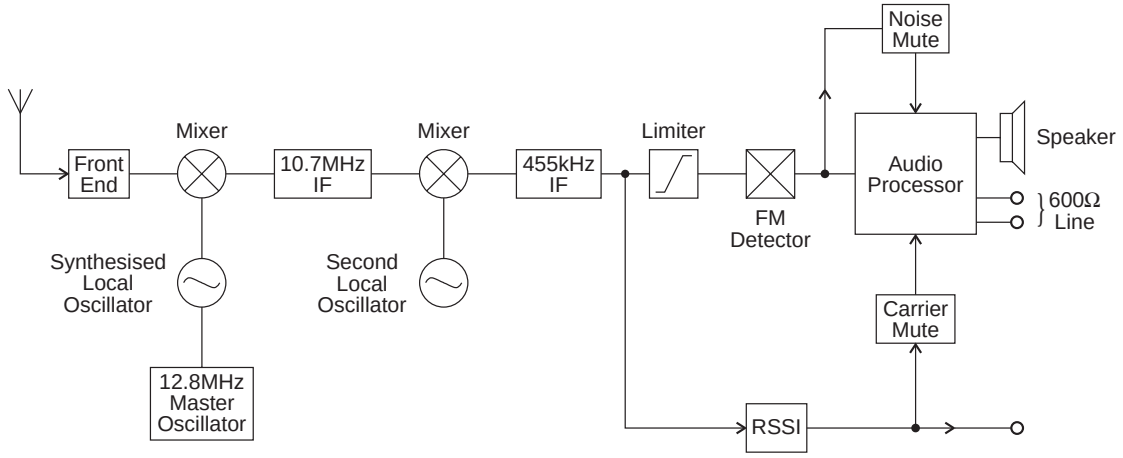
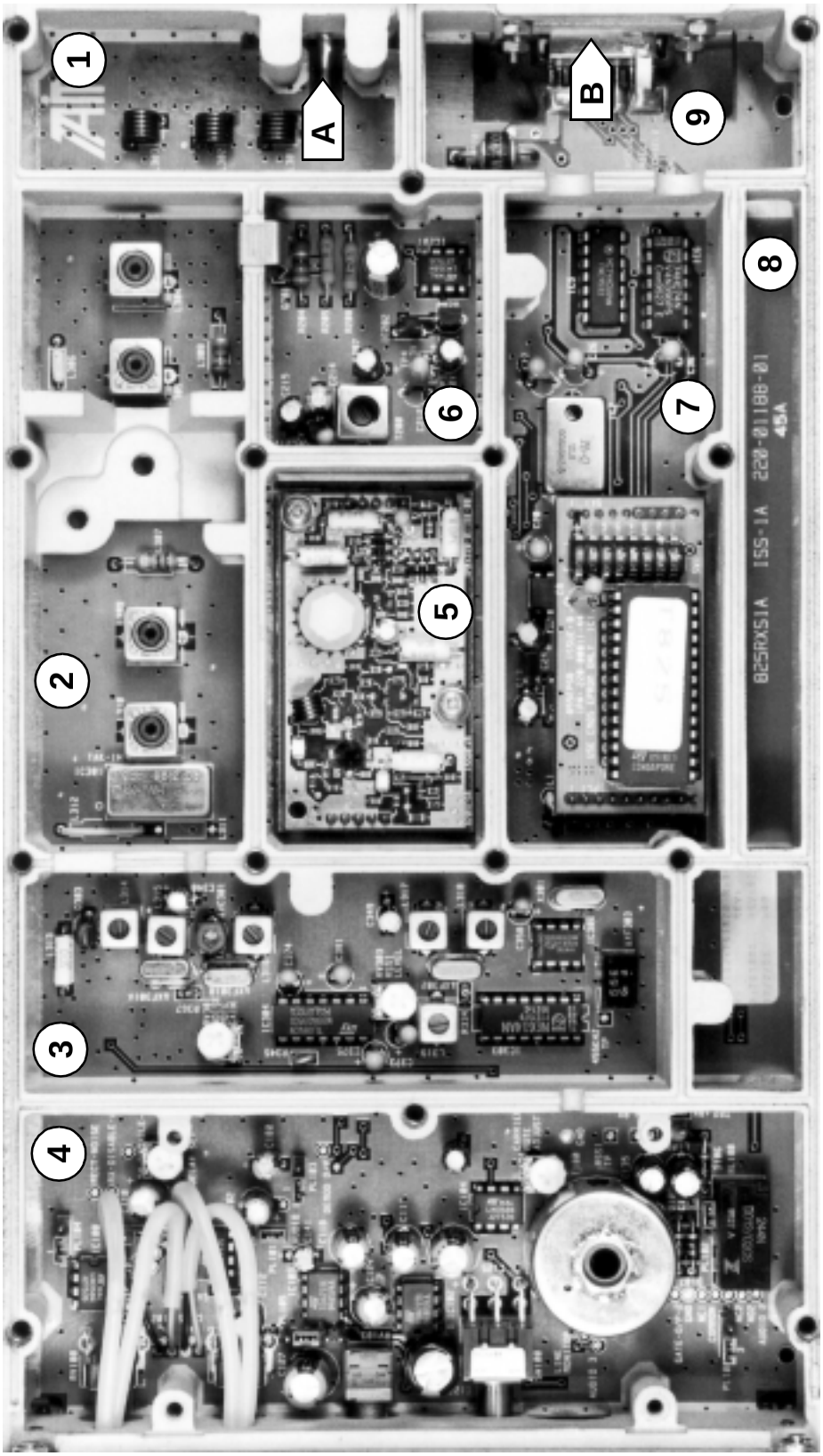


Figure 2.1 T825 High Level Block Diagram

The T825 receiver consists of a number of distinct stages:

- front end
- mixer
- synthesised local oscillator
- IF
- audio processor
- mute (squelch)
- regulator circuits
- received signal strength indicator (RSSI).

These stages are clearly identifiable in Figure 2.1. Figure 2.2 shows the location of the main circuit blocks on the PCB. Refer to the circuit diagrams in Section 6 for further detail.



Key:

1 low pass filter
2 front end
3 receiver
4 audio processor
5 VCO
6 regulator
7 synthesiser
8 duct for cabling to extra D-range (if fitted)
9 D-range
A RF in
B D-range connector (incl. audio out & DC in - refer to Section F1.2)

Figure 2.2 T825 Main Circuit Block Identification

2.2 Receiver Front End

(Refer to the receiver and audio processor circuit diagrams in Section 6.)

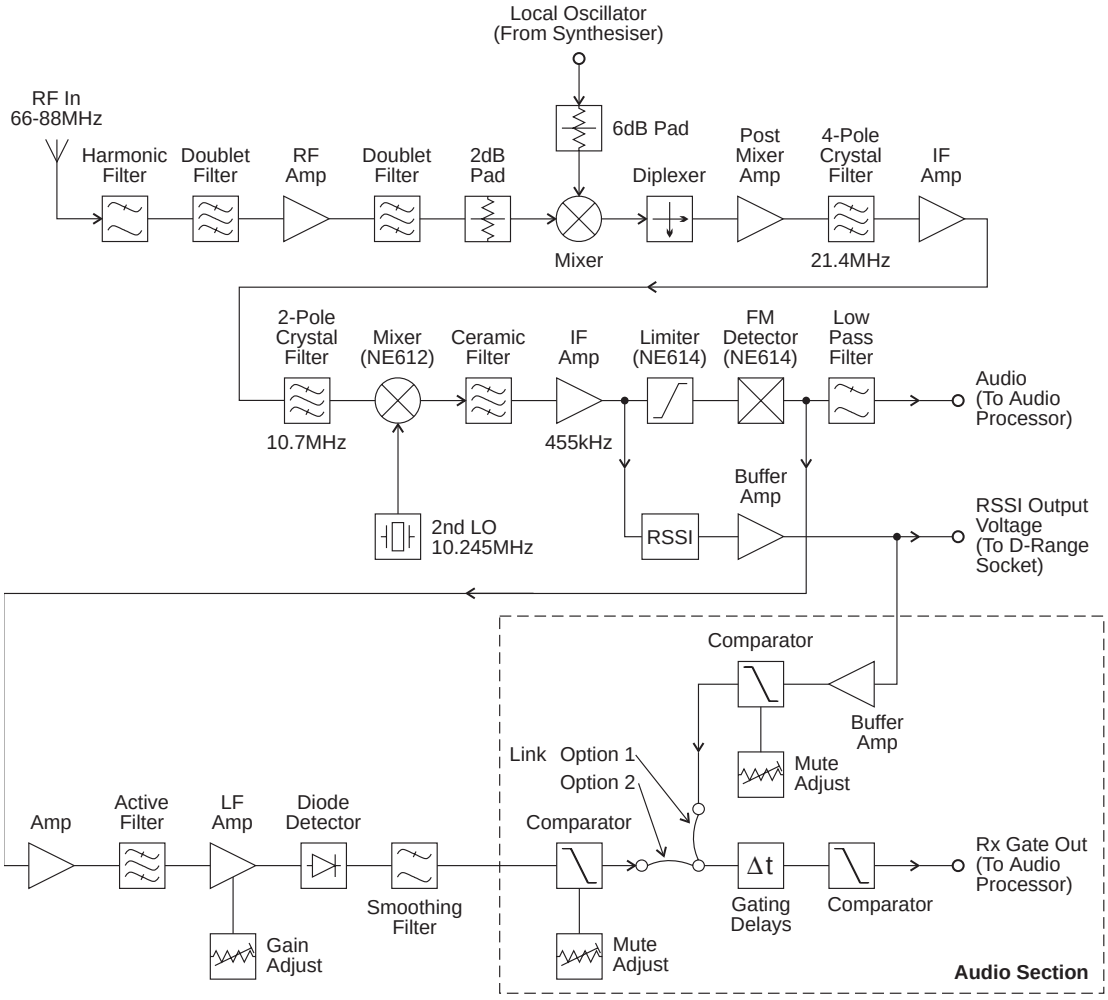


Figure 2.3 T825 Front End, IF and Mute Block Diagram

The incoming signal from the N-type antenna socket is fed through a 7-pole, low pass filter with a cut frequency of approximately 91MHz. This low loss filter (typically less than 0.5dB over 66-88MHz) provides excellent immunity to interference from high frequency signals.

The signal is then further filtered, using a notched doublet (L304, L305) which provides exceptional image rejection, before being amplified by approximately 12dB (Q302). The signal is then passed through a further doublet (L309, L310) before being presented to the mixer via a 2dB attenuator pad[1].

Each sub-block within the front end has been designed with 50 ohm terminations for ease of testing and fault finding. The overall gain from the antenna socket to the mixer input varies from 3-5dB.

1. The 2dB attenuator pad is not fitted to sets produced after March 1993.

2.3 Mixer

(Refer to the receiver circuit diagram in Section 6 and Figure 2.3.)

IC301 is a high level mixer requiring a local oscillator (LO) drive level of +17dBm (nominal). The voltage controlled oscillator (VCO) generates a level of +22dBm (typical) and this is fed to the mixer via a 6dB attenuator pad. A diplexer[1] terminates the IF port of the mixer in a good 50 ohms, thus preventing unnecessary intermodulation distortion.

2.4 IF Circuitry

(Refer to the receiver circuit diagram in Section 6 and Figure 2.3.)

Losses in the mixer are made up for in a tuned, common gate, post mixer amplifier (Q303). Several stages of amplification and filtering are employed in the IF circuitry. The first crystal filter is a 4-pole device (&XF301) which is matched into 50 ohms on both its input and output ports. This stage is followed by a two-stage amplifier which is designed as a 50 ohm block, after which the signal is mixed down to 455kHz with the second local oscillator (10.245MHz).

The 455kHz signal is filtered using a six-pole ceramic filter (&XF303) before being limited and detected.

The second IF mixer, limiter, detector and RSSI is in a 16-pin IC (IC303). Quadrature detection is employed, using L319, and the recovered audio on pin 7 of IC303 is typically 0.3V p-p for 60% system deviation. The audio is then passed through a low pass filter and buffer before being passed to the audio processor and noise mute.

1. Not fitted to sets produced after March 1993.

2.5 Noise Mute (Squelch)

(Refer to the receiver circuit diagram in Section 6 and Figure 2.3.)

The noise mute operates on the detected noise outside the audio bandwidth. An operational amplifier in IC304 is used as an active band pass filter centred on 70kHz to filter out audio components. The noise spectrum is then further amplified in a variable gain, two-stage amplifier (Q306 & Q307) with additional filtering. The noise is then rectified (D301) and filtered to produce a DC voltage proportional to the noise amplitude. The lowest average DC voltage corresponds to a high RF signal strength and the highest DC voltage corresponds to no signal at the RF input.

The rectified noise voltage is compared with a threshold voltage set up on RV100, the front panel mute potentiometer. Hysteresis is introduced by the feedback resistor (R106) to prevent the received message from being chopped when the average noise voltage is close to the threshold. R111 and R110 determine the mute opening and closing times. The mute control signal at pin 7 of IC100 is used to disable the speaker and line audio outputs. The speaker output can be separately enabled for test purposes by operating the front panel mute disable switch, SW100.

The mute control line is available on pad 101 (Rx gate out) for control of external circuitry. A high (9V) on pad 101 indicates that the audio is disabled and a low (0V) indicates that a signal above the mute threshold level is being received.

The audio can also be disabled using the "Rx-disable" inputs, pads 100 or 113, having connected the "Rx-disable" link between pins 1 & 2 of PL100. An adjustable time delay (RV101) is provided on these lines. In order to disable the audio, either pad must be pulled to 0V.

The red front panel LED (D102) indicates the status of the mute circuit. When a signal above the mute threshold is received, the LED is illuminated. An undedicated relay is provided (RL100) for transmitter keying or other functions and this can be operated from the mute line by linking PL102.

2.6 Carrier Mute

(Refer to the receiver circuit diagram in Section 6 and Figure 2.3.)

A high level carrier mute facility is also available. The RSSI (refer to Section 2.10) provides a DC voltage proportional to the signal strength. This voltage is compared with a preset level, set up on RV104, and may be linked into the mute timing circuit using PL104. PL104 selects either the noise mute or the carrier mute. From this point both mute circuits operate in the same manner, using common circuitry.

2.7 Audio Processor

(Refer to the audio processor circuit diagram in Section 6.)

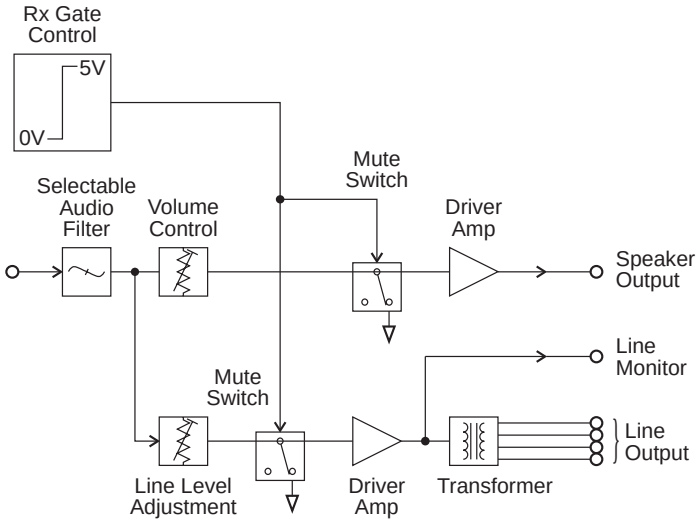


Figure 2.4 T825 Audio Processor Block Diagram

The recovered audio on pin 7 of IC303 is processed in a third order elliptic active filter to give the required response. Linking (PL101 & PL103) is available to give either a flat or de-emphasised audio response, with de-emphasis giving a 6dB / octave roll off. The output of IC101 is split to provide separate paths for the speaker and line outputs.

The speaker volume is set using the front panel volume knob (RV103) and the line level is set using the recessed potentiometer (RV102). The signals are passed to audio drive amplifiers IC102 and IC103. Under muted conditions the inputs of these amplifiers are shunted to ground via transistors Q105 and Q106 respectively.

The audio output of IC102 has a DC component which is removed by C122, and this then drives a speaker directly. The output of IC103 is fed into a line transformer to provide a balanced 2-wire or 4-wire, 600 ohm output.

2.8 Power Supply And Regulator

(Refer to the regulator circuit diagram in Section 6.)

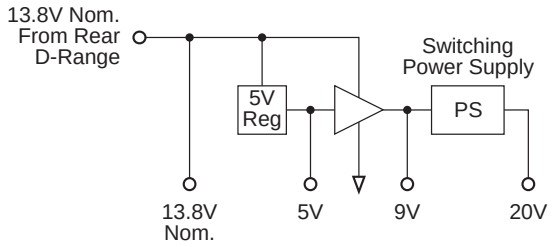


Figure 2.5 T825 Power Supply And Regulator Block Diagram

The T825 is designed to operate off a 10.8-16V DC supply (13.8V nominal). A 5.3V regulator (IC202) runs directly off the 13.8V rail, driving much of the synthesiser circuitry. This is used as the reference for a DC amplifier (IC201, Q200 & Q201) which provides a medium current capability 9V supply. A switching power supply, based on Q202 and Q203, runs off the 9V supply and provides a low current capability +20V supply. This is used to drive the synthesiser loop filter (IC4), giving a VCO control voltage of up to 20V. The 13.8V supply drives both output audio amplifiers without additional regulation.

2.9 Synthesised Local Oscillator

(Refer to the synthesiser circuit diagram in Section 6 and the VCO circuit diagram in Part E.)

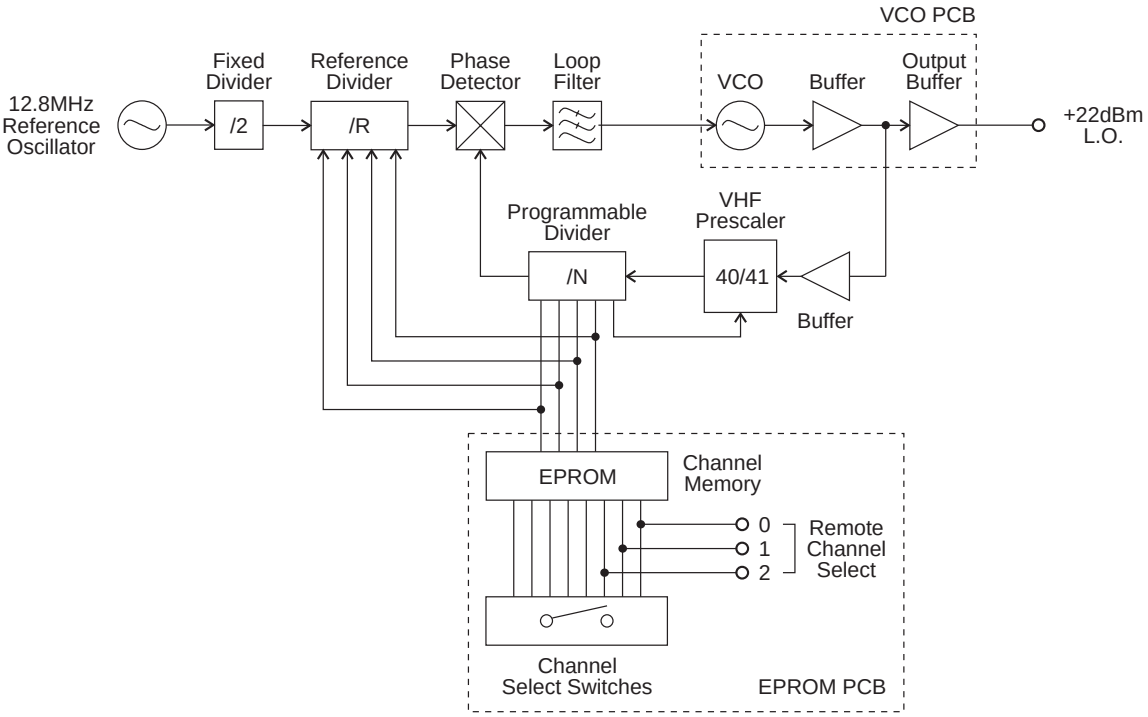


Figure 2.6 T825 Synthesiser Block Diagram

The synthesiser employs a phase-locked loop (PLL) to lock a VCO to a given reference frequency.

A master oscillator at 12.8MHz (IC2) is buffered, divided by two and then divided down to 6.25kHz or 5kHz within the synthesiser IC (IC3). A buffered output of the VCO is fed to a programmable divider, comprising a VHF prescaler (IC1) and a divider internal to IC3. These two signals are applied to the phase detectors in IC3. A digital phase detector (PDB) provides rapid coarse tuning of the VCO until the phase error is within the range of the high gain sample and hold detector (PDA). The phase detector outputs are passed through an active loop filter (IC4a) which produces a DC voltage between 0 and 20V to tune the VCO. This VCO control line is further filtered to attenuate noise and spurs. As the control line voltage increases, the VCO frequency also increases.

The division ratio of the programmable divider is stored within EPROM memory (IC1). Up to 128 frequencies can be stored within the memory and are addressable using the internal DIP switches. Three of the address lines are also available for external frequency control via an extra D-range connector at the rear of the chassis. A change of state of any of these three lines (CH SEL 0-2) commences a programming cycle during which the frequency data in the EPROM is down-loaded to a divider within IC3. 32 bits of data are loaded in eight 4-bit words.

The VCO transistor (Q1) operates in a common source configuration, with an LC tank circuit coupled between its gate and drain to provide the feedback necessary for oscilla-

tion. The VCO control voltage from the loop filter (IC4) is applied to the varicaps (D1-D6) to facilitate tuning within a 2MHz band of frequencies. A trimcap (VC1) is used for coarse tuning of the VCO. The output from the oscillator circuit drives a cascode amplifier stage (Q2, Q3) which supplies +10dBm (typically) to a further stage of amplification, Q5. This is the final amplifier on the VCO PCB, and delivers +22dBm (typically) to the receiver mixer input pad.

A low level "sniff" is taken from the input to Q5 and used to drive the divider buffer for the VHF prescaler (IC1). The prescaler divide ratio is 40/41.

The VCO operates at the actual frequency required by the first mixer, i.e. there are no multiplier stages.

The VCO frequency spans from 76.7-98.7MHz. The VCO is tuned to 10.7MHz above the desired receive frequency to produce a 10.7MHz IF signal on the output of the mixer.

2.10 Received Signal Strength Indicator (RSSI)

(Refer to the receiver circuit diagram in Section 6.)

The RSSI provides a DC voltage proportional to the signal level at the receiver input and is an on-chip function of IC303. Buffering and temperature compensation are provided by IC304 and the voltage is available at the rear D-range connector.

The RSSI also provides the capability for high level signal strength muting, which may be selected on PL104 (refer to Section 3.3). The mute threshold may be set between -125dBm and -70dBm at RV104.

